SERVICE TEXT
FILE NO. 176-096

TOSHIBA

DIGITAL SYNTHESIZER TUNER

ST-S20

SUBJECT: DIGITAL SYNTHESIZER TUNER BASIC EXPLANATION

CONTENTS

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983

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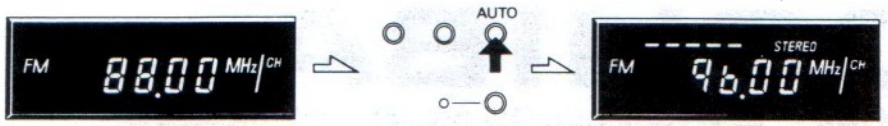

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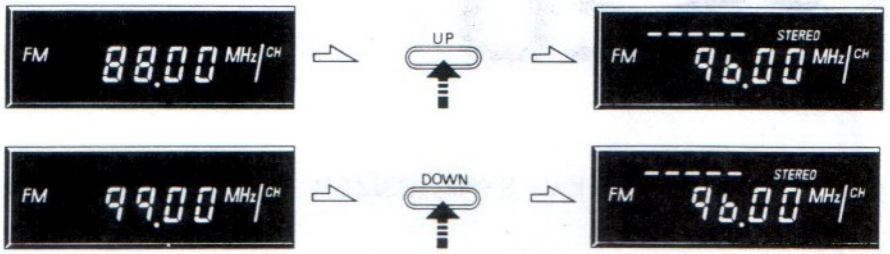

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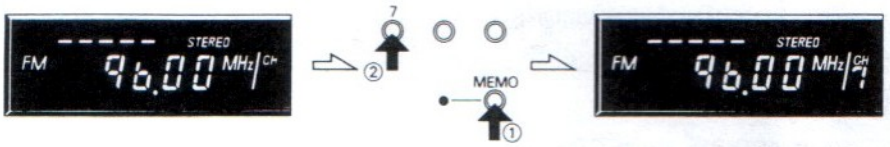

4

• Preset tuning

Figure 1.

3. BLOCK DIAGRAM

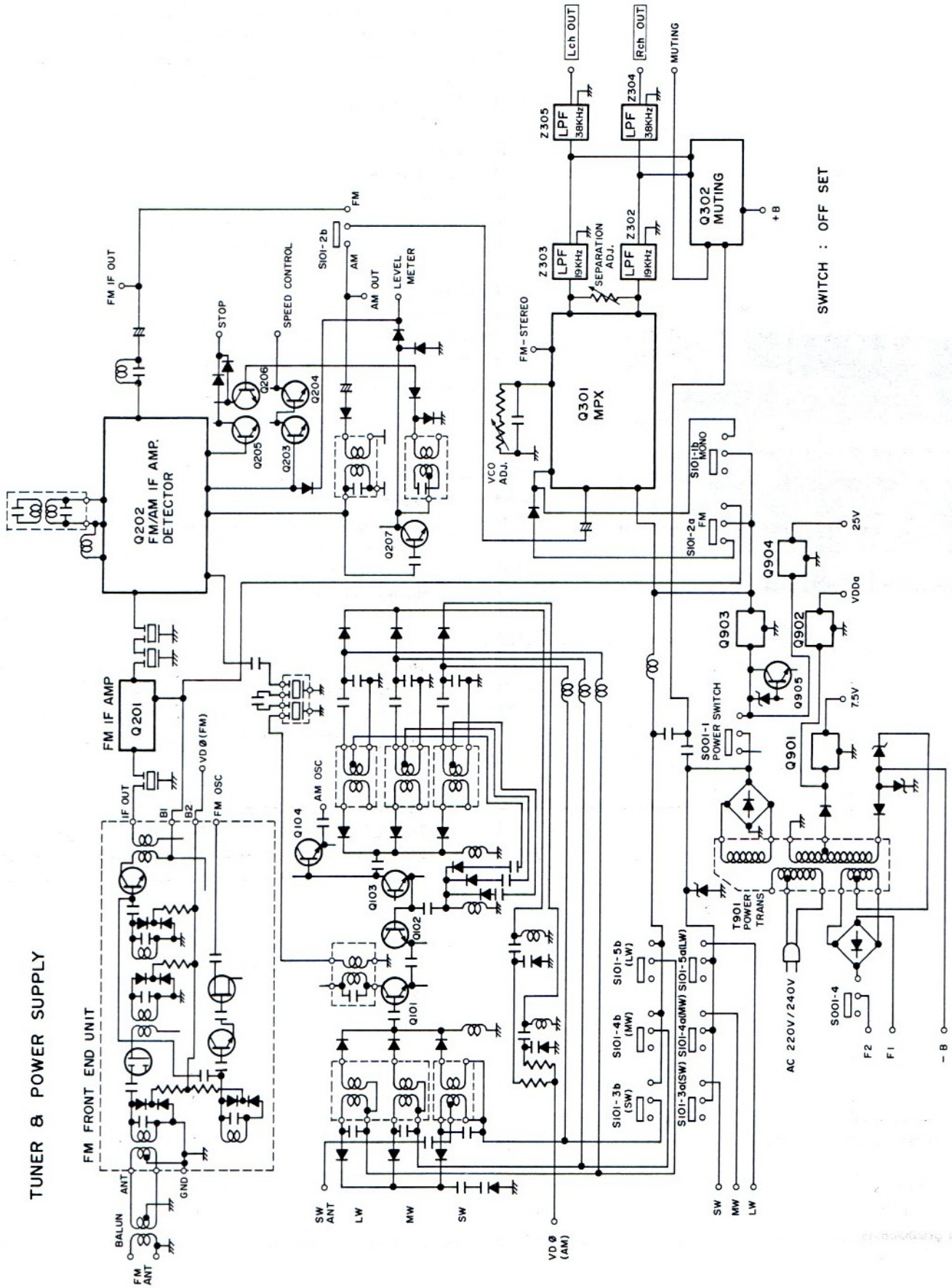

Figure 3.

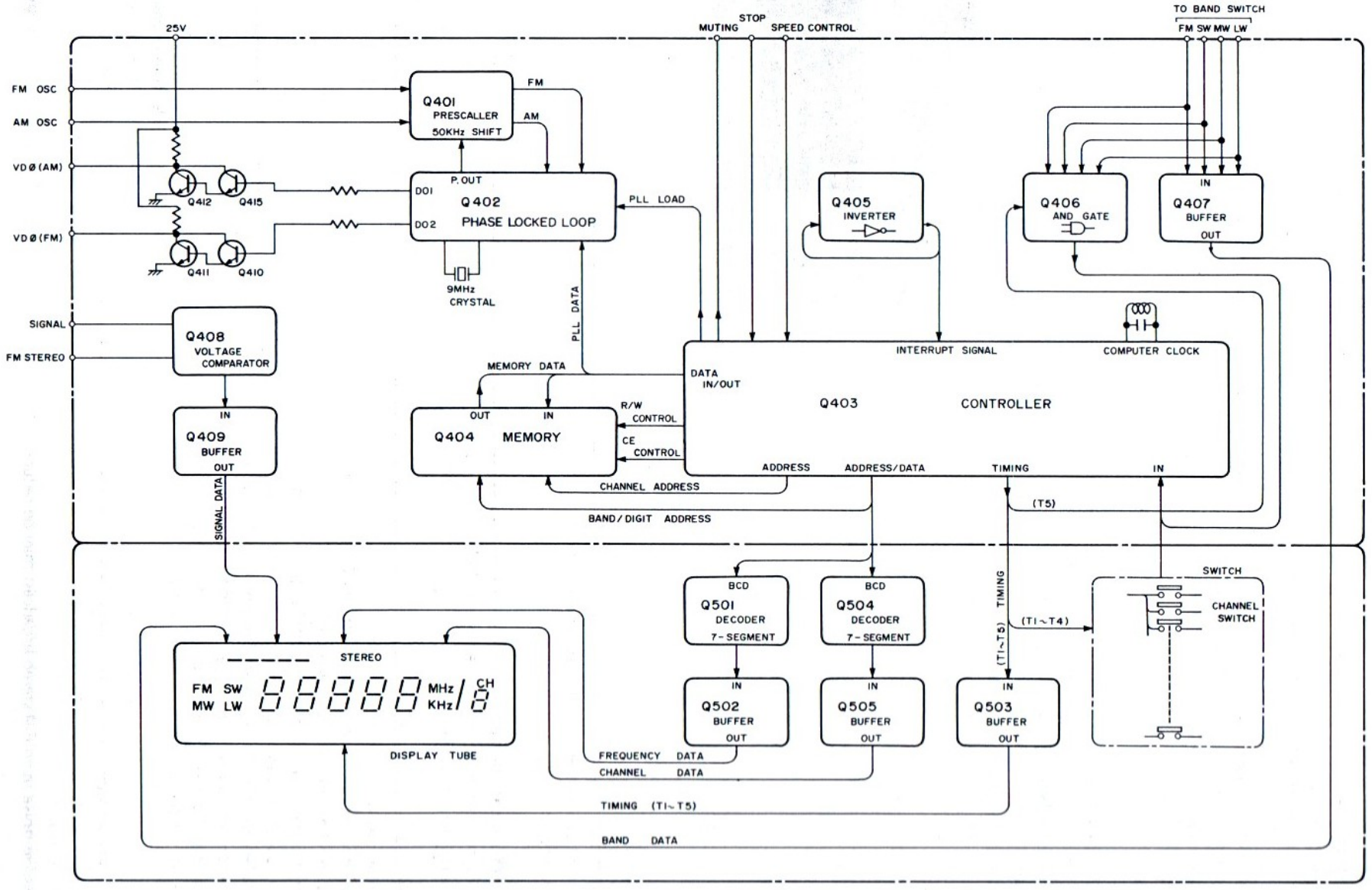
25V
MUTING
STOP
SPEED CONTROL
TO BAND SWITCH
FM SW MW LW
FM OSC
AM OSC
VDØ(AM)
VDØ(FM)
Q401
PRESCALLER
50KHz SHIFT
FM
AM
Q412
Q415
Q411
Q410
P.OUT
DO1
DO2
Q402
PHASE LOCKED LOOP
PLL LOAD
9MHz
CRYSTAL
PLL DATA
Q405
INVERTER
Q406
AND GATE
IN
Q407
BUFFER
OUT
SIGNAL
FM STEREO
Q408
VOLTAGE
COMPARATOR
INTERRUPT SIGNAL
COMPUTER CLOCK
MEMORY DATA
DATA
IN/OUT
Q403
CONTROLLER
IN
Q409
BUFFER
OUT
OUT
IN
Q404
MEMORY
R/W
CONTROL
CE
CONTROL
ADDRESS
ADDRESS/DATA
TIMING
IN
CHANNEL ADDRESS
(T5)
BAND/DIGIT ADDRESS
SIGNAL DATA
BCD
Q501
DECODER
7-SEGMENT
BCD
Q504
DECODER
7-SEGMENT
TIMING
(T1~T5)
(T1~T4)
SWITCH
CHANNEL
SWITCH
STEREO
FM SW
MW LW
MHz
KHz
CH
DISPLAY TUBE
IN
Q502
BUFFER
OUT
IN
Q505
BUFFER
OUT
IN
Q503
BUFFER
OUT
FREQUENCY DATA
CHANNEL DATA
TIMING (T1~T5)
BAND DATA

Figure 4.

2. OPERATING CONTROLS

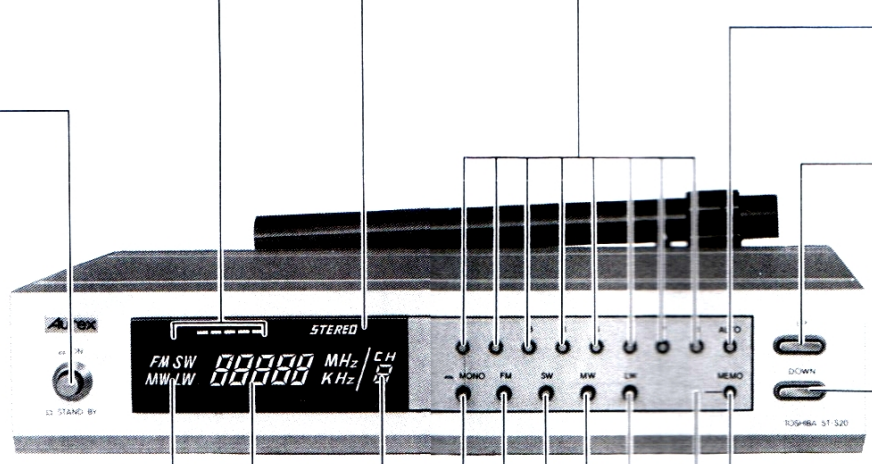

Figure 2.

① [STEREO]
FM stereo indicator
Lights up when an FM stereo station has been tuned.

② **Signal level indicator**
These lamps light up from left to right the stronger stations being indicated by more lamps. If 4 or 5 lamps fail to come on for a local station, check antenna connections and direction.

③ **Power switch**
When the power switch is turned on, a frequency will be appear immediately in the display. This frequency is the last tuned station before power was turned off.
If none of the radio band selector buttons ⑧ are depressed, an FM frequency will be displayed but no sound will be heard.

④ **Band display**
This displays the band, of the radio band selector button 2 depressed at that time.

⑤ **Digital frequency display**
The tuned frequency in all 4 bands (LW/MW/SW/FM) is displayed here in digital form.

⑥ [CH]
Channel display
When one of the preset tuning buttons ⑨ is depressed its channel number is displayed here.
When the radio band selector buttons ⑧ are switched, the channel display ⑥ will go off. The frequency displayed is that of the last station tuned in that band. If the preset tuning button ⑨ of that station is now depressed (assuming the station is in the memory), the channel number will appear in the display.

⑦ **Mono push-button**
This button selects either the stereo mode or the mono (monaural) mode.
Excessive noise in an FM stereo broadcast may be reduced by pressing this button.

⑧ **Radio band selector buttons**
Choose your program source by pressing one of these function buttons.

LW:	for LW radio broadcasts
MW:	for MW radio broadcasts
SW:	for SW radio broadcasts
FM:	for FM radio broadcasts

⑨ **Preset tuning buttons (1 – 8)**
Once the memory button ⑬ has been pressed, press one of these buttons immediately afterward to store the frequency of the desired station in the memory. To recall the frequency at a later date, simply press the corresponding tuning button.

⑩ [AUTO]
Auto tuning button
For tuning in the FM and MW bands, press this button to "scan" the frequencies automatically. The scanning motion will stop once a broadcast station is tuned.

⑪ [MANUAL UP]
Manual up button
The frequency is likewise increased stepwise by this manual up button, the change being continuous if the button remains depressed.

⑫ [MANUAL DOWN]
Manual down button
The frequency is changed (reduced) one step at a time every time this button is pressed. If the button remains depressed, the frequency will change continuously until the button is released again.

⑬ [MEMO]
Memory push-button
To store the frequency of any desired station in the memory, first press this button. The memory indicator lamp ⑭ lights up to indicate that the memory is ready to accept the frequency.

⑭ **Memory indicator lamp**
This LED lamp lights up for approx. 5 seconds only when the memory button ⑬ is pressed. Presetting of the desired station must be performed before this lamp goes out.

4. SYNTHESIZER METHODS

The basic principles involved in the frequency synthesizer tuning method employed in the ST-S20 are outlined below.

4-1 COMPOSITION

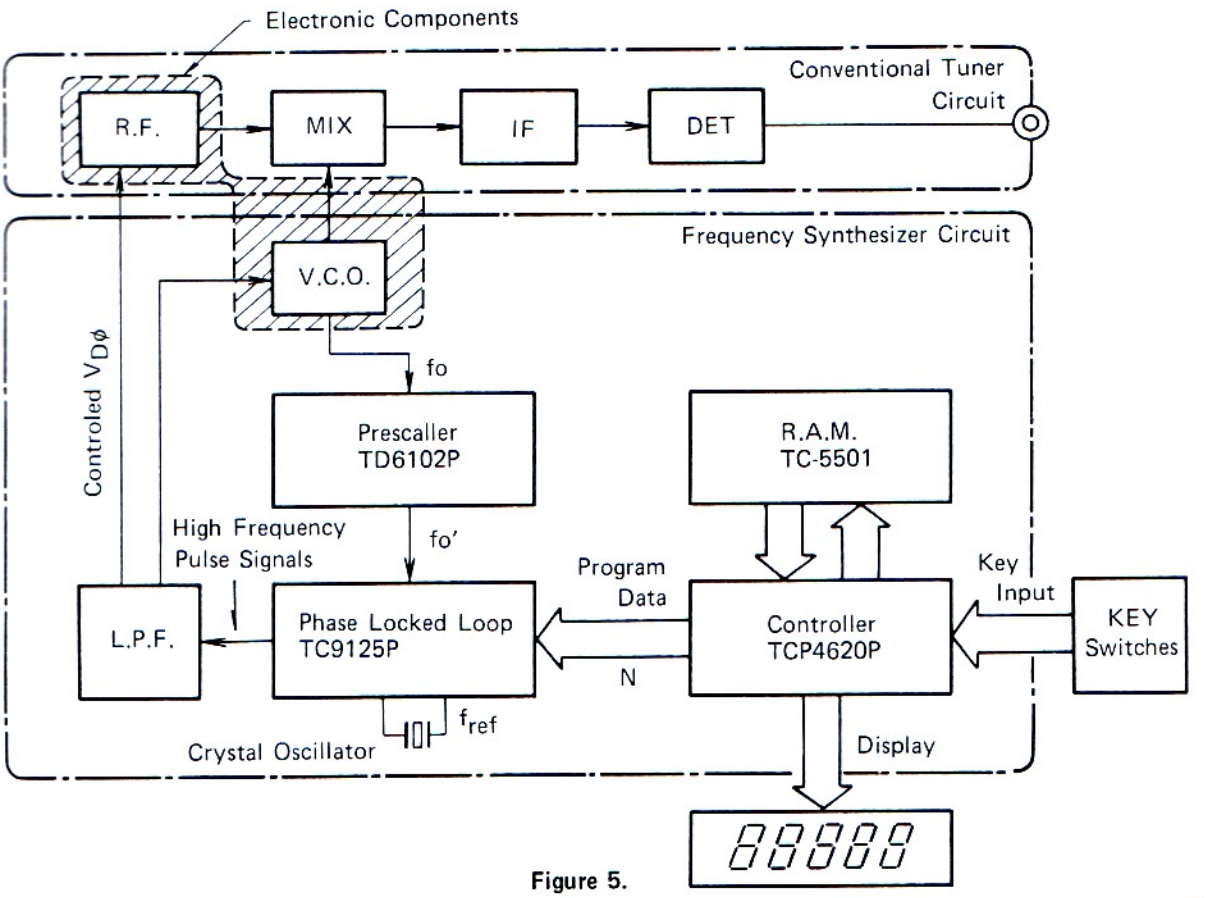

Figure 5.

The above block diagram outlines the major component parts in the ST-S20 frequency synthesizer tuning circuit. These parts are briefly described below.

- The circuits enclosed in the upper section make up a conventional tuning circuit. Note, however, that the RF is an electronic circuit in this case.
- The VCO (Voltage Controlled Oscillator) frequency fo is divided by the prescaler (TD6102P) into frequency f'o. The frequency division ratio is 1/8 for FM and 1/1 for AM.
- The phase locked loop (TC9125P) then divides this f'o by the command data N from the controller, and compares the resultant f'o/N with f'ref obtained by dividing the reference frequency fref (different division ratio employed in each band).
- As a result of this comparison, high frequency pulse signals are generated in order to reduce fo if f'o/N is less than f'ref, or increase fo if f'o/N is greater than f'ref.
- These pulse signals are then passed via the low-pass filter, converted into an analog voltage (by smoothing out into a DC voltage) which is subsequently applied to the VCO and other tuning circuit elements.
- By repeating this process continually at very high speed, a very constant and accurate fo oscillator frequency is obtained.
- The TMP4620P controller reads data generated by externally operated key switches and band selector, and then translates the data into a form usable by each block (PLL, DISPLAY, RAM) in order to control the operation of other circuits.
- The TC5501P RAM (Random Access Memory) stores different data ready for retrieval according to commands from the controller.

This frequency synthesizer tuning method is thus capable of synthesizing and controlling frequencies more accurately than was possible in conventional tuning circuits.

4-2 BASIC TUNING OPERATION

An example of basic synthesizer tuning operations when tuning to an actual broadcast frequency has been outlined below with the use of typical figures.

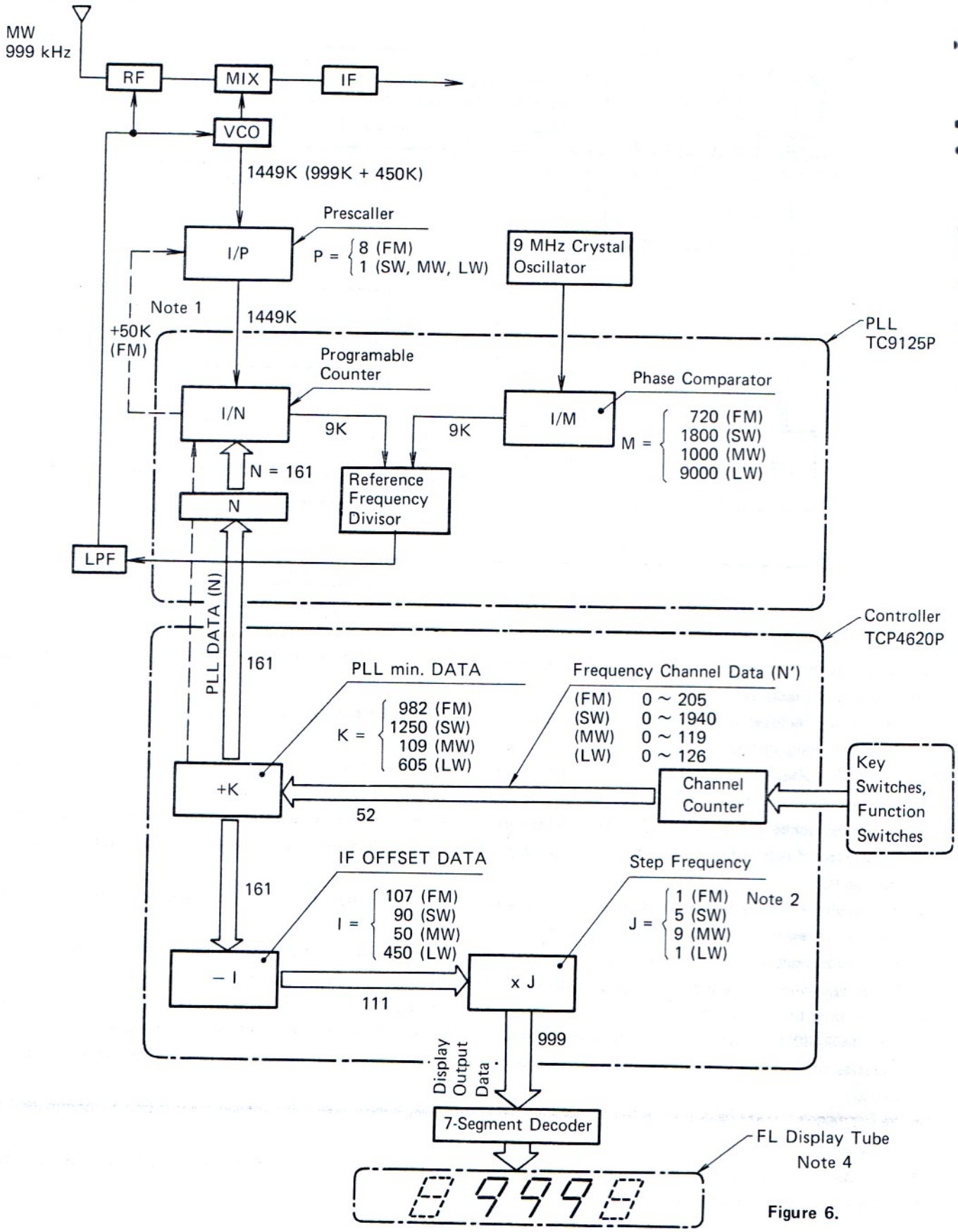

Figure 6.

Fig. 6 above outlines the flow of data. The example shown is for reception of 999 kHz in the MW band.

utlined below

- When the relevant key switch is operated, the channel counter in the controller is set to "52". (The operator will not see this "52" displayed – "999" which corresponds to channel 52 will be seen instead).
  [By counting up in 9 kHz steps from fmin = 531 kHz (channel 0), f = 999 kHz (channel 52) will be reached].
- This "52" is converted in the controller into PLL data and also display data.
  PLL data ..... "161"
  Display data ..... "999" Note 3
- The "161" PLL data is set in the PLL programable counter.
- It is assumed here that the local oscillator is oscillating in the 1499 kHz (999 + 450 kHz) region (a small amount of divergence from this frequency will not present any problems). This signal is then passed through the prescalar (1/1 in MW band) and applied to the PLL programable counter.
- In this counter, the frequency is divided by N (= 161) already set in the counter, thereby obtaining a 9 kHz signal which is subsequently applied to the phase comparator.
- The 9 kHz signal is then compared (phase comparison) with a 9 kHz reference signal obtained by dividing the 9 MHz output frequency from the highly stable crystal oscillator circuit.

PLL
TC9125P

- The phase comparator output is passed through the low-pass filter and converted into an analog voltage to be used in the control of the tuning voltage.

Note 1: The reception frequency is shifted by 50 kHz by special operation during FM reception. For further details, refer to the section on the prescalar.

Note 2: Since FM frequencies are changed up and down in 100 kHz steps while SW, MW and LW frequencies are read in kHz units, J = 1 is used for FM only.

Note 3:

PLL data $52 + \overset{K}{\boxed{109}} = 161$

Display data $\left(52 + \overset{K}{\boxed{109}} - \overset{I}{\boxed{50}}\right) \times \overset{J}{\boxed{9}} = 999$

Controller
TCP4620P

Note 4: Frequencies are displayed in the ST-S20 in a fluoroscent display tube. Note that basic operation is quite different to that involved in LED displays.

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Fluorescent Display Tube Operational Principles

Outline of fluorescent display tube:

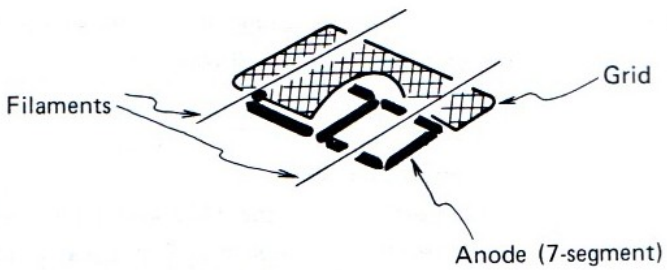


Figure 7.

Illumination principle

- Thermal electrons are discharged from the surface when a current is passed through the filament.
- When the voltage applied to the anode and grid is positive in reference to the filaments, these thermal electrons are accelerated through the grid onto the anode, resulting in excitation of the fluorescent medium and subsequent illumination of the corresponding segments.
- When the applied voltage is negative in reference to the filaments, the thermal electrons do not reach the anode. Hence, the corresponding segments will not light up.

The display method employed in the ST-S20 is a dynamic drive method where the whole grid is divided into 5 parts, and each part is illuminated separately on a time sharing basis.

Basic circuit diagram

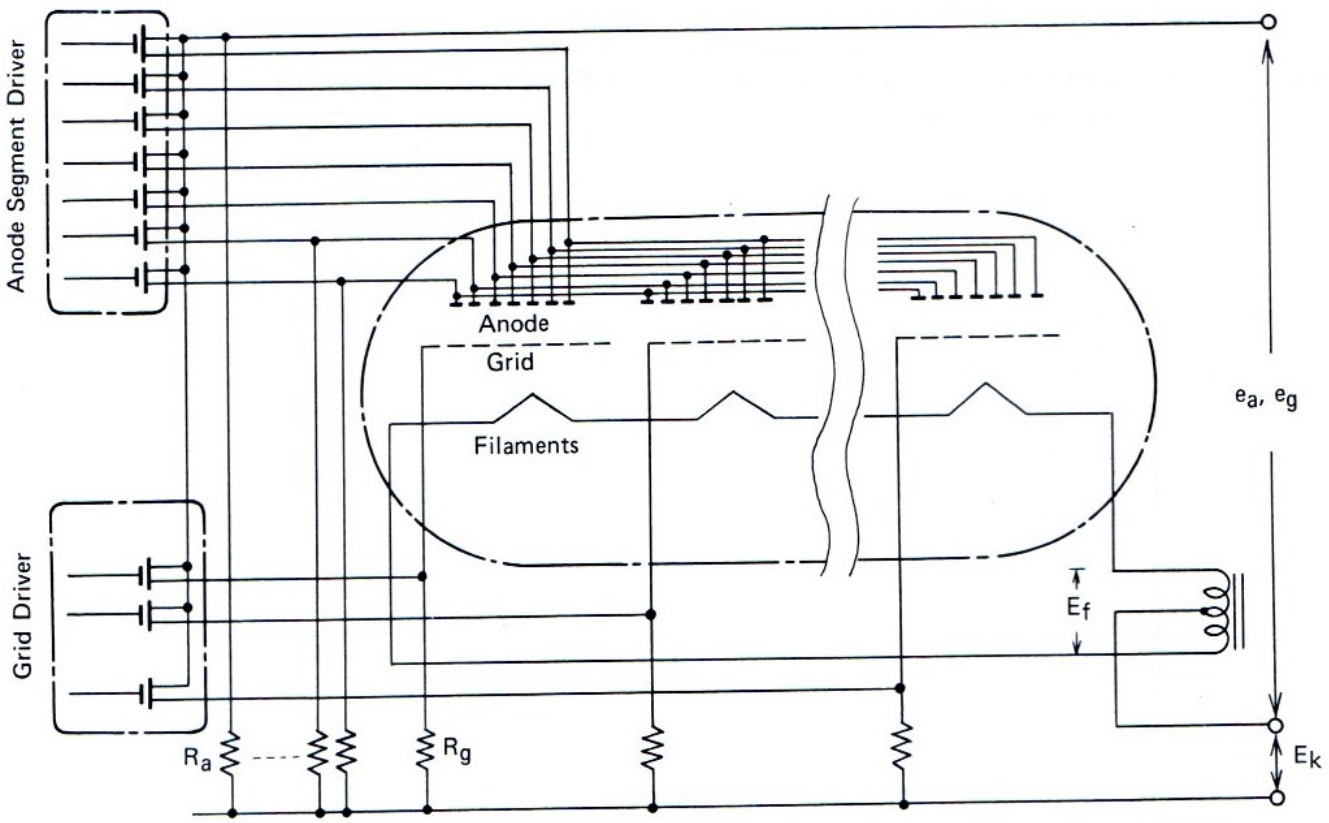


Figure 8.

- An E_f AC voltage is applied to the filaments, and e_a (anode voltage) and e_g (grid voltage) (which lie in the positive direction from the E_f center point potential) are applied to the anode and grid respectively.
- E_k is a bias voltage used to extinguish the fluorescent illumination. This is achieved by reducing the anode and grid voltages below the negative peak value of the E_f voltage. E_k is applied to the anode and grid via R_a and R_g respectively.

Handling precautions

The service life of the fluorescent display tube is determined by the degree of vaporization of the filament electron emission substance. And the rate of vaporization is controlled by the filament temperature (i.e. filament voltage). The filament voltage is therefore a critical factor, and it is of the utmost importance that no voltage in excess of the prescribed voltage be applied. If an overvoltage is applied, the life of the fluorescent tube will be shortened in a very brief moment. Since the filament voltage is obtained directly from the power transformer as an AC voltage, the ST-S20 must never be used with any other power voltage except the designated voltage rating.

4-4 PHASE LOCKED LOOP (TC9125P) OPERATION

Note: This PLL IC is based on the same operational principles as TC-9123, but differs in set data in order to operate in combination with TCP-4620.

The 5 major component parts in this IC are listed below.

1) Reference frequency divider
2) Programable counter
3) Phase comparator
4) P_{OUT} control
5) Data latch

These are outlined in the following block diagram.

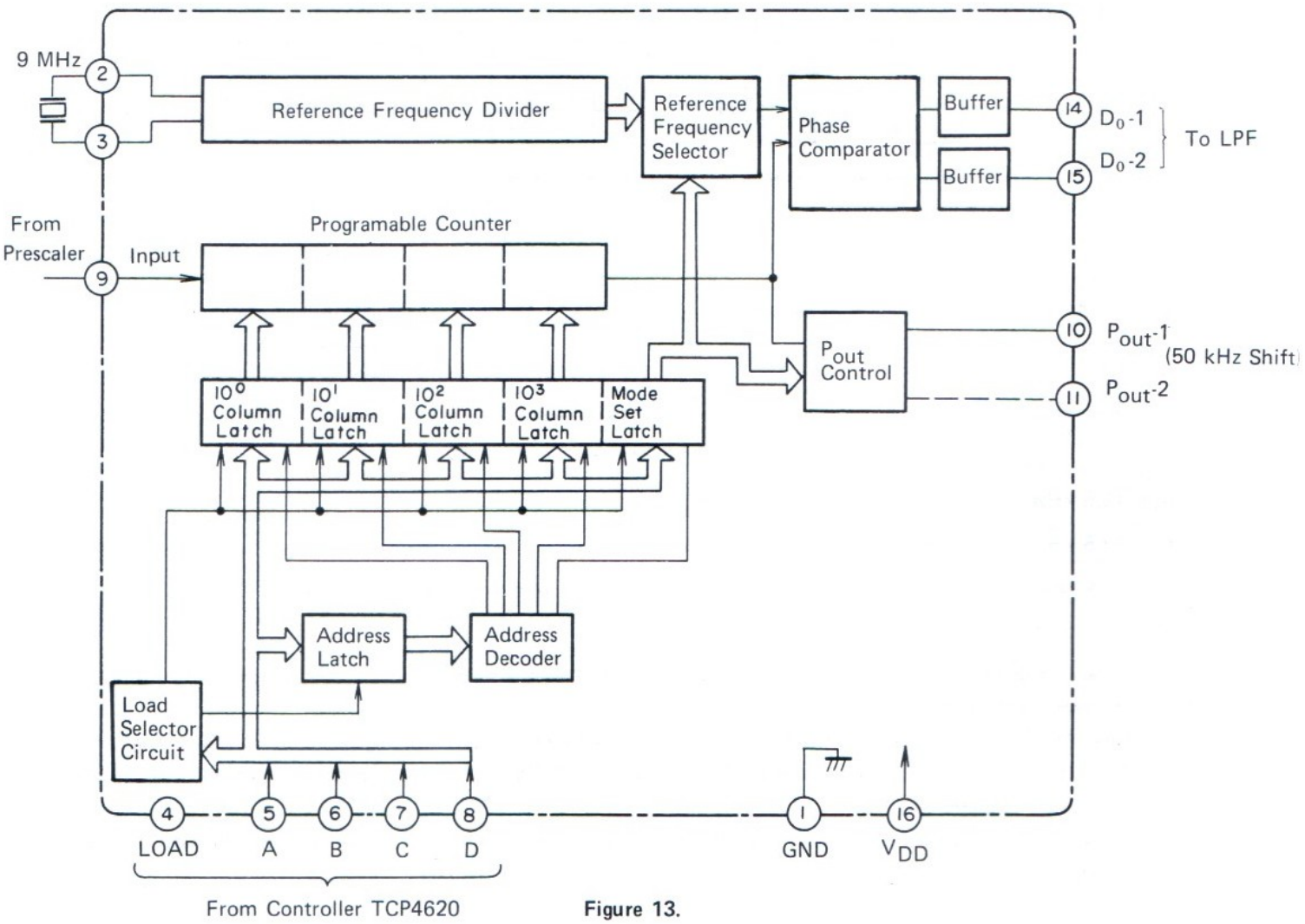


Figure 13.

(1) Reference Frequency Divider

- The reference frequency is obtained by dividing the output of the externally connected 9 MHz crystal oscillator. The 4 different reference frequencies (note) for the 4 different bands (listed in the table below) are selected by mode commands from the controller).

Mode	FM	SW	MW	LW
Frequency divisor	720	1800	1000	9000
Reference frequency (kHz)	12.5	5.0	9.0	1.0

Figure 14.

(2) Programable Counter

- The programable counter is a frequency divider capable of controlling the frequency divisor according to the program data (corresponds to N in Fig. 6) supplied by the TCP4620P controller. This counter handles up to 4 digits (16 bits) in columns A, B, C and D.
- The frequency divisors for the signal frequencies in each broadcast band are listed in the following table.

Band	Frequency		Frequency Change per Step	Channels	Frequency Divisor	
	f_{min}	f_{max}			Lower	Upper
FM	87.5 MHz	108.0 MHz	100 kHz	0 ~ 205	982	1187
SW	5.800 MHz	15.500 MHz	5 kHz	0 ~ 1940	1250	3170
MW	531 kHz	1602 kHz	9 kHz	0 ~ 119	109	228
LW	155 kHz	281 kHz	1 kHz	0 ~ 126	605	731

Figure 15.

- The divided frequency output is then passed to the phase comparator for phase comparison with the reference frequency (See (3) on page 14.).
- This output is also passed to the P_{OUT} control circuit, appearing at the programable counter output terminals P_{OUT}-1 and P_{OUT}-2 connected to the prescaler 50 kHz shift terminal for use in the 50 kHz shift operation during FM reception mode (See (4) on page 15.).
- Furthermore, the frequency divisor N applied in serial binary form one digit at a time from pin nos. ⑤, ⑥, ⑦ and ⑧, is temporarily stored in parallel in the internal latch circuit before being passed in proper sequence to the programable counter by the address decoder. It goes without saying that this kind of data is transferred under control of the TCP4620 controller.

Note: Although there appear to be 205 channels for FM reception, there are actual twice as many channels available for reception since each channel may be shifted by 50 kHz (with the same frequency divisor N) (See section 4-3 Prescaler for further details).

(3) Phase Comparator

- The phase of the programable counter output signal is compared with the phase of the reference frequency divider output signal in this comparator stage. The output signal is applied to the VCO via a low-pass filter in such a way as to bring the phase of both signals into conformity with each other.
- The 2 output terminals Do-1 ⑭ and Do-2 ⑮ are connected to separate low-pass filters for AM (SW, MW, LW) and FM respectively. And with a Pch/Nch C-MOS FET combination in the output, try state outputs are also possible.

Condition	Pout-1 Pout-2
Øpc behind Øref	L level
Øpc = Øref	High Impedance
Øpc ahead of Øref	H level

Figure 16.

Øpc : programable counter output signal phase
Øref : reference frequency divider output signal phase

(4) P_{OUT} Control Circuit

- The output status of the P_{OUT}-1 and P_{OUT}-2 programable counter frequency divider output terminals is controlled by this control circuit.
- The control command applies the mode set data from the TCP4620 controller to pin nos. ⑤ ~ ⑧, the resultant output being determined according to the type of command.
- This mode set data (A5, B5, C5)(note 2) and the corresponding P_{OUT}-1 output status is listed in the following table.

Band	Mode set data			Reference frequency (kHz)	P_{OUT}-1	
	A5	B5	C5			
LW	0	0	0	1	Sig.	
SW	1	0	0	5	Sig.	
MW	0	1	0	9	Sig.	
FM	0	0	1	12.5	1	*
FM	1	0	1	12.5	Sig.	*

Sig. : Programable counter output signal
1 : H level maintained

Figure 17.

Note 1: This terminal is not used in the ST-S20.
Note 2: In addition to P_{OUT} control, this mode set data is also employed in the selection of the different reference frequencies for the different bands.

- As can be seen from the above table, FM reception is possible in 50 kHz steps. The method employed is described briefly below.
  The astericks (*) in Fig. 17 denote that the P_{OUT}-1 status may be changed without altering the reference frequency. The following chart illustrates this with actual broadcasting frequencies.

Frequency Divisor N	A5	B5	C5	P_{OUT}-1	50K Shift	VCO Frequency	Reception Frequency
⋮							⋮
1007	0	0	1	1	●	100.70 MHz	90.00 MHz
1007	1	0	1	Sig.	○	100.75	90.05
1008	0	0	1	1	●	100.80	90.10
1008	1	0	1	Sig.	○	100.85	90.15
1009	0	0	1	1	●	100.90	90.20
1009	1	0	1	Sig.	○	100.95	90.25
1010	0	0	1	1	●	101.00	90.30
1010	1	0	1	Sig.	○	101.05	90.35
1011	0	0	1	1	●	101.10	90.40
⋮							⋮

Control signal

○ denotes a frequency shift (of 50 kHz)
● denotes that no shift has occurred

Figure 18.

So if data is transferred from the controller as algorithms in the sequence shown in Fig. 17, reception will be possible in steps of 50 kHz. The TCP4620P controller in the ST-S20 has been designed to perform this function. For additional details, refer to the section on the controller (4-5).

(5) Data Latch

- In order to apply data (4 digits for frequency divisor N, and 1 digit for mode set data) from the TCP4620P controller in serial form from pin nos. ⑤ ~ ⑧, the TC9125P has been equipped with an internal 4 bit x 5 latch circuit.

LOAD signal

- Before discussing the data latch, a few words will be said about the LOAD signal.

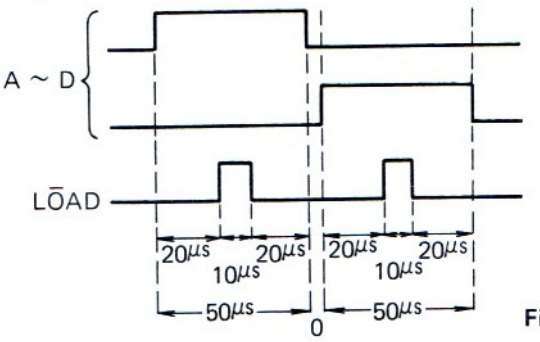


Figure 19.

Fig. 19 above shows the relation between the A ~ D signals and the LOAD signal. The LOAD signal designates read in of the A ~ D signal data. Data is read in when LOAD is "1", and is stored when LOAD is "0". The reason for this is to eliminate unstable sections and use the stable central section for writing in when switching the A, B, C and D data, thereby minimizing the possibility of mis-operation.

- To resume the data latch explanation, refer back to Fig. 18.
  The binary input data on A ~ D is first classified according to whether the value is 0 ~ 9 or 11 ~ 15.

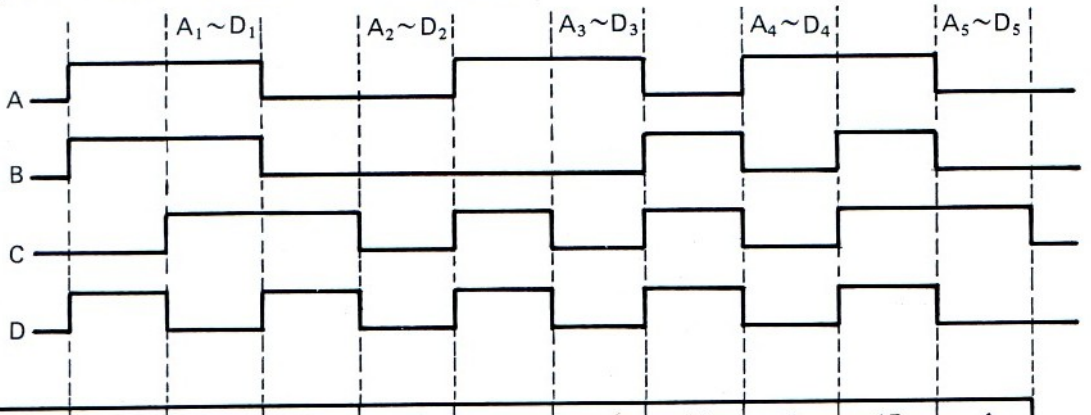
If 11 ~ 15

The LOAD signal from the load selection circuit is applied to the address latch where the data is subsequently stored. Then the data latch (10^0 ~ 10^3 latch or mode set latch) designated by the data is designated by the address latch.

If 0 ~ 9

The LOAD signal from the load selection circuit is applied to the data latch where the data is subsequently stored.

- Hence, by transferring this 0 ~ 9 and 11 ~ 15 data alternately, 4 digits of programable counter set data and 1 digit of mode set data may be applied.
- For example, when FM 100.00 MHz is tuned, the input data will be as follows.
  An input signal of 100.00 MHz means that the programable counter frequency divisor N will be 1107 (See Fig. 6).



Binary code value	11	7	12	0	13	1	14	1	15	4
Address designation	10^0 digit		10^1 digit		10^2 digit		10^3 digit		Mode set	
Data set		7		0		1		1		⇧

No 50 kHz shift in FM mode (see Figure 17)

Figure 20.

Hence, the following data will be transferred:—

"1107" to the programable counter

"FM" to the reference frequency selection circuit

"No output pulse" to P_{OUT} control

4-5 CONTROLLER (TC4620P-4103) OPERATION

The role of the controller is the overall control of the data flow by combined control of the prescaler (4-3) and PLL circuit (4-4). Hence, all operations are controlled by command signals issued by this controller stage.
The major types of operation may be summarized as follows.

1) Read in of externally operated key switch and band switch inputs.
2) Input and output of data to and from external memory (RAM) (i.e. write in and read out).
3) Display commands and data transfer to DISPLAY.
4) Command and data transfer to PLL.
5) Auto tuning data handling.

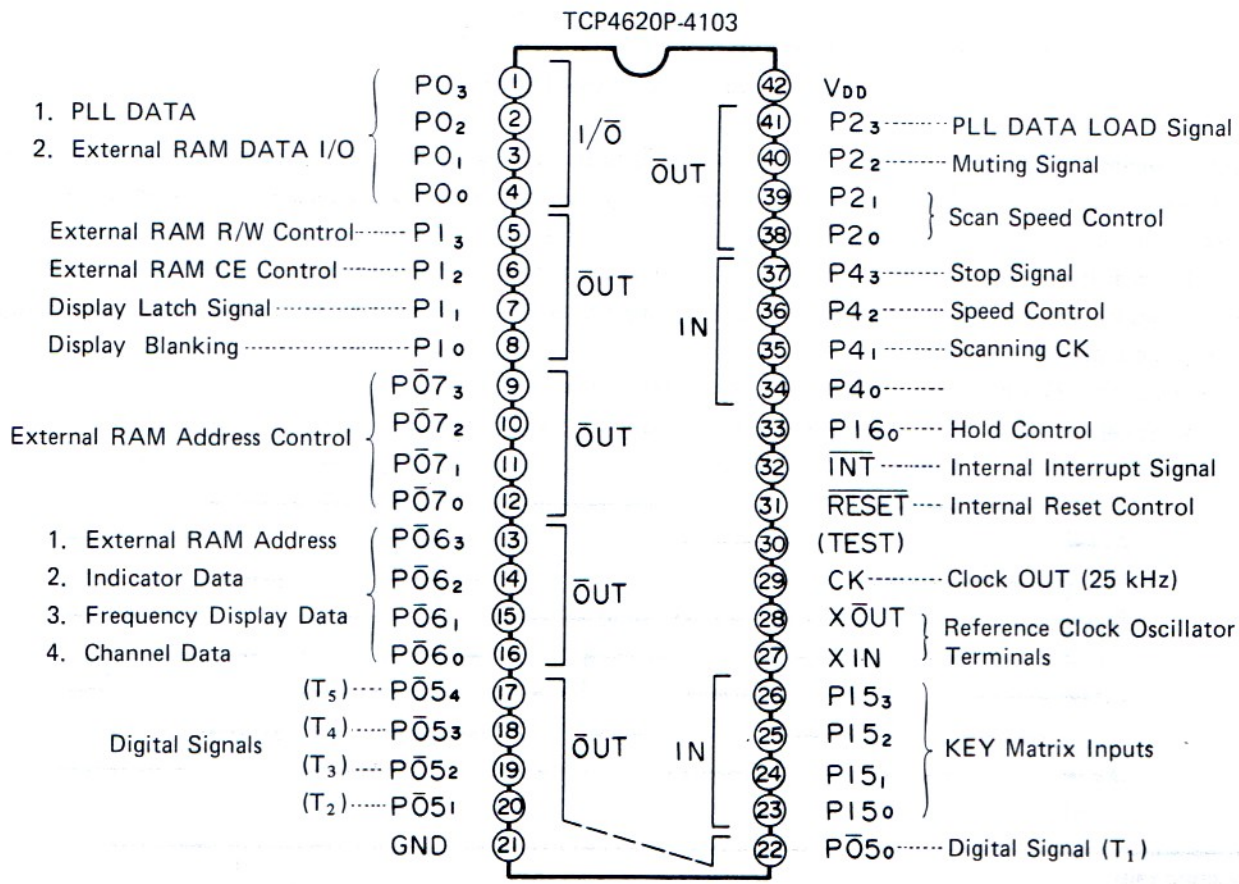
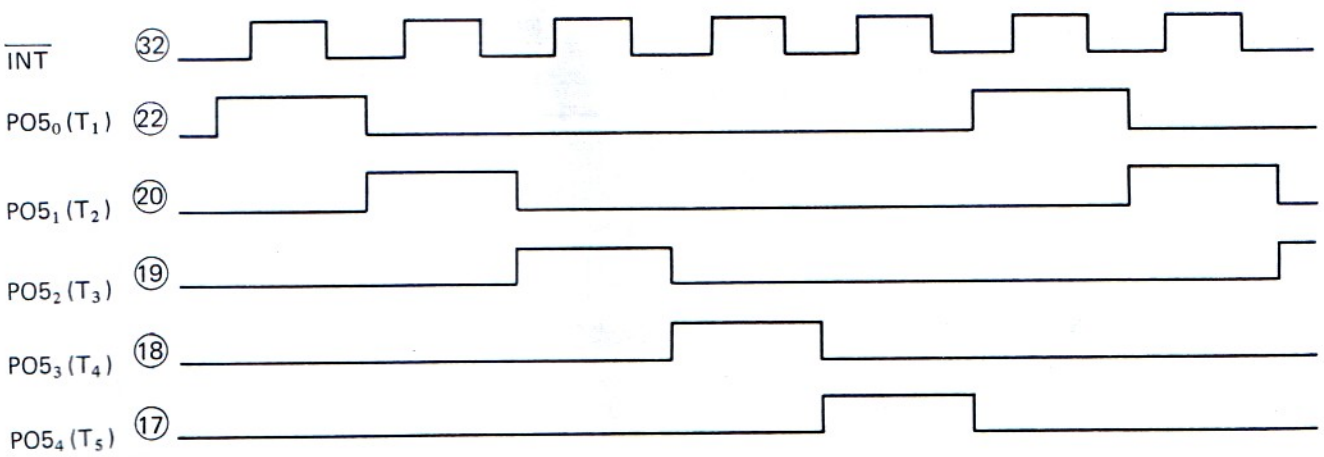


Figure 21.

8-1. Switch Input Read In

- The timing signals from pin nos. (22), (20), (19), (18) and (17) are passed via the externally operated switch (key, band) and applied to the (23), (24), (25), (26) matrix inputs for the controller to identify which switch has been operated. The following output commands are determined on the basis of this identification.
- The timing signals are outlined in the following diagram.



Note that INT is repeated every 3.5msec.

- The switching circuit is outlined below.

Figure 22.

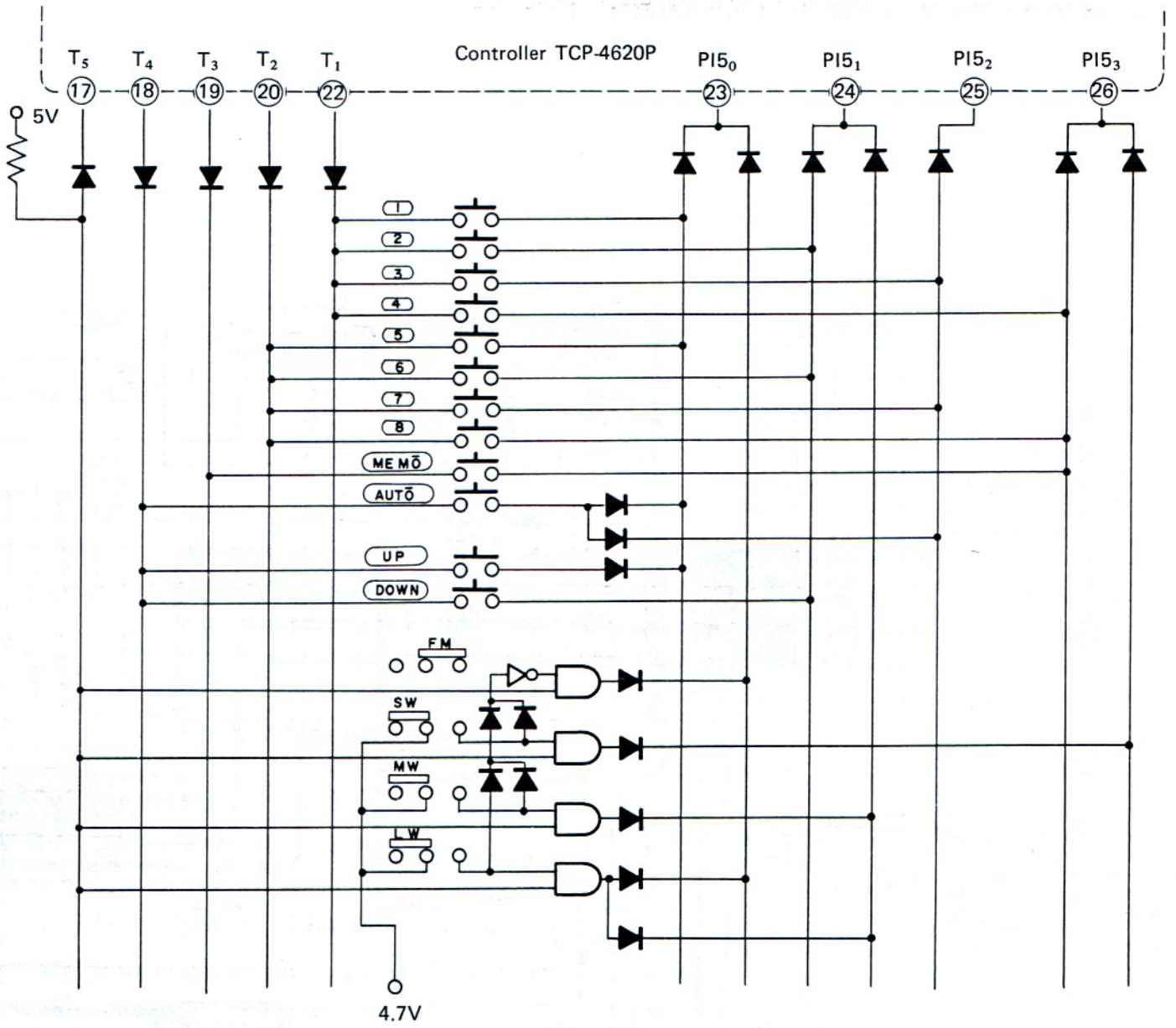


Figure 23.

Note: [1], [2], ... [8], [MEMO], [AUTO], [UP] and [DOWN] are simple push-button key switches. The band selector is a 4-step push-button switch. The above diagram shows the case for FM reception.

- Timing $T_1 \sim T_5$ and the PI5 (23) ~ (26) input status are summarized in the following table.

Pin No.	T_1				T_2				T_3	T_4			T_5			
$PI5_0$ (23)	1	0	0	0	1	0	0	0	0	1	0	1	1	0	0	1
$PI5_1$ (24)	0	1	0	0	0	1	0	0	0	0	1	0	0	0	1	1
$PI5_2$ (25)	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0
$PI5_3$ (26)	0	0	0	1	0	0	0	1	1	0	0	0	0	1	0	0
Meaning of Key Input	1	2	3	4	5	6	7	8	MEMO	UP	DOWN	AUTO	FM	SW	MW	LW

Figure 24.

Key input meaning for each timing is identified by the controller, and the corresponding command is passed to the relevant circuits by shifting to the next program.

EXTERNAL MEMORY DATA WRITE IN AND READ OUT

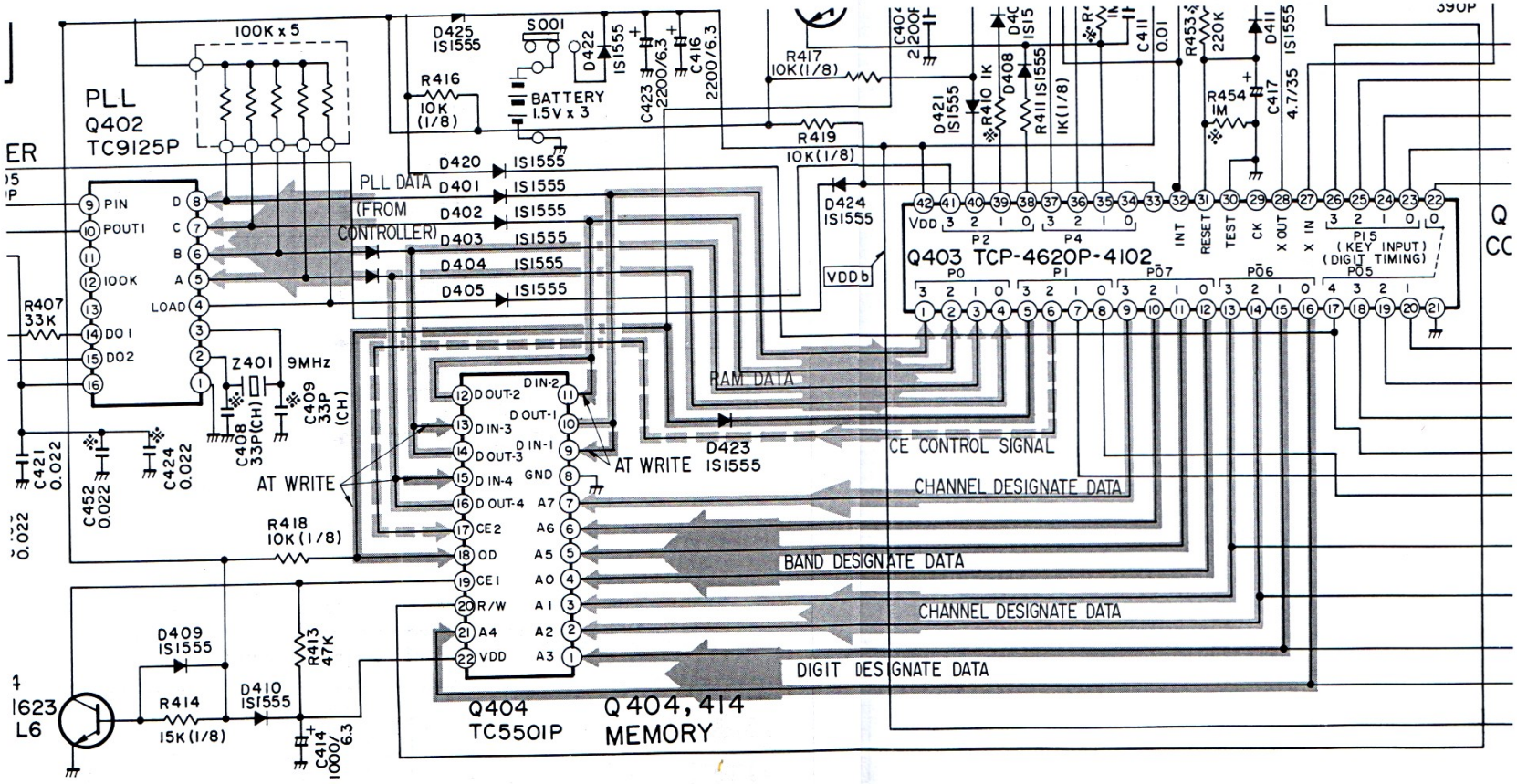


Figure 25.

8-2. External MEMORY Data Write In and Read Out

The following description of MEMORY read out and write in is made in reference to Fig. 25.

(i) Read out from MEMORY

1. According to key switch operation (band, channel) band designation data is transferred to MEMORY via pin nos. ⑨, ⑬ and ⑭, while channel designation data (for channels 1 to 8) is transferred via pin nos. ⑩, ⑪ and ⑫.
2. The corresponding memory content is applied to the controller via pin nos. ①, ②, ③ and ④ as 4-digit frequency channel data (RAM data) in accordance to the CE (chip enable) control signal from pin no. ⑥ while digits ($10^0 \sim 10^3$) are being designated at pin nos. ⑮ and ⑯.
3. This data is then converted into PLL data.
4. The PO ports (pin nos. ①, ②, ③ and ④) are put into output mode.
5. Data is transferred to the PLL via pin nos. ①, ②, ③ and ④ in accordance with the LOAD signal from pin no. ㊶.

(ii) Write into MEMORY

1. Pin nos. ①, ②, ③ and ④ are put into output mode.
2. Band is designated by pin nos. ⑨, ⑬ and ⑭, while channel is designated by pin nos. ⑩, ⑪ and ⑫.
3. Pin no. ⑤ is put into write status (H level).
4. The last-channel data (presently displayed frequency) in the controller is written in as 4-digit RAM data according to the digit designation on pin nos. ⑮ and ⑯, and the CE signal on pin no. ⑥.

- The above description may be summarized as shown in the following diagram.

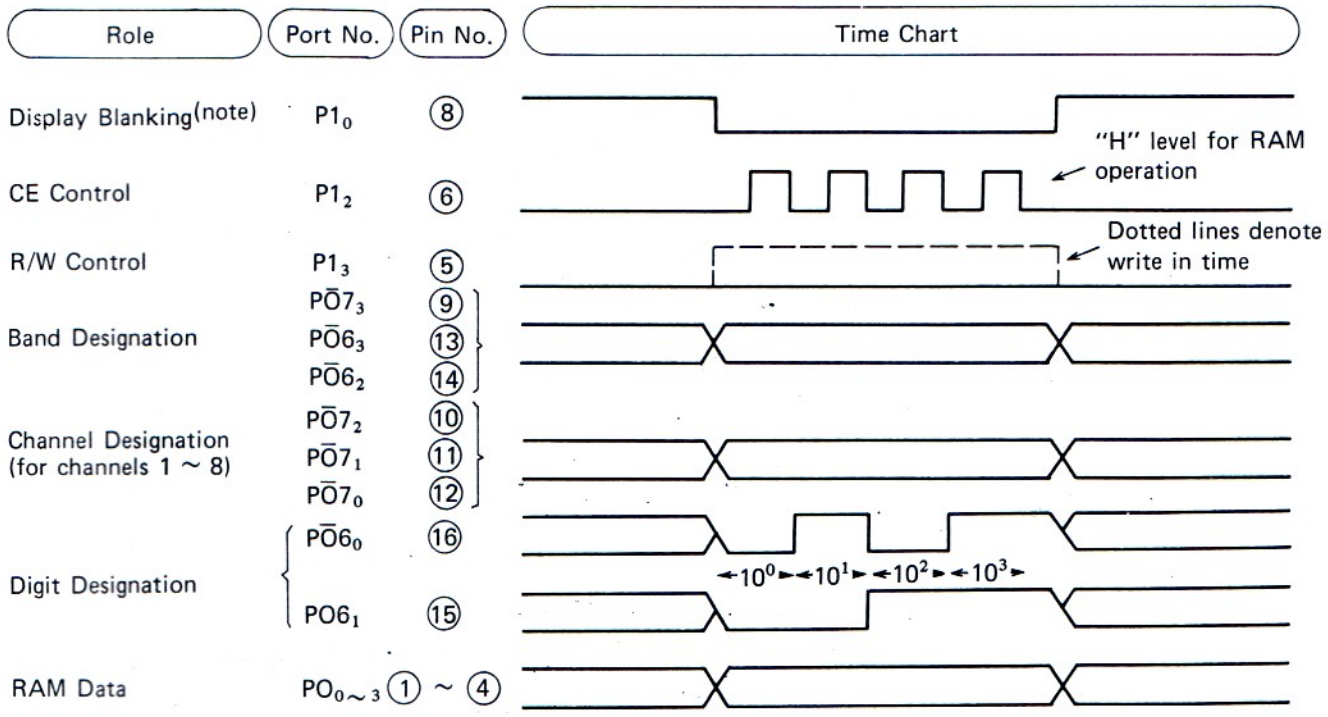


Figure 26.

Note: The display is blanked out by the blanking signal during this operation.

- The various output data and corresponding meanings are as follows.

Band designation data

$PO6_2$	⑭	0	1	1	0
$PO6_3$	⑬	0	1	0	1
$PO7_3$	⑨	0	0	0	1
Meaning		FM	SW	MW	LW

Digit designation data

$PO6_0$	⑯	0	1	0	1
$PO6_1$	⑮	0	0	1	1
Meaning		10^0 digit	10^1 digit	10^2 digit	10^3 digit

Channel designation data

$PO7_0$	⑫	0	1	0	1	0	1	0	1
$PO7_1$	⑪	0	0	1	1	0	0	1	1
$PO7_2$	⑩	0	0	0	0	1	1	1	1
Meaning		1CH	2CH	3CH	4CH	5CH	6CH	7CH	8CH

Figure 27.

DATA TRANSFER TO DISPLAY

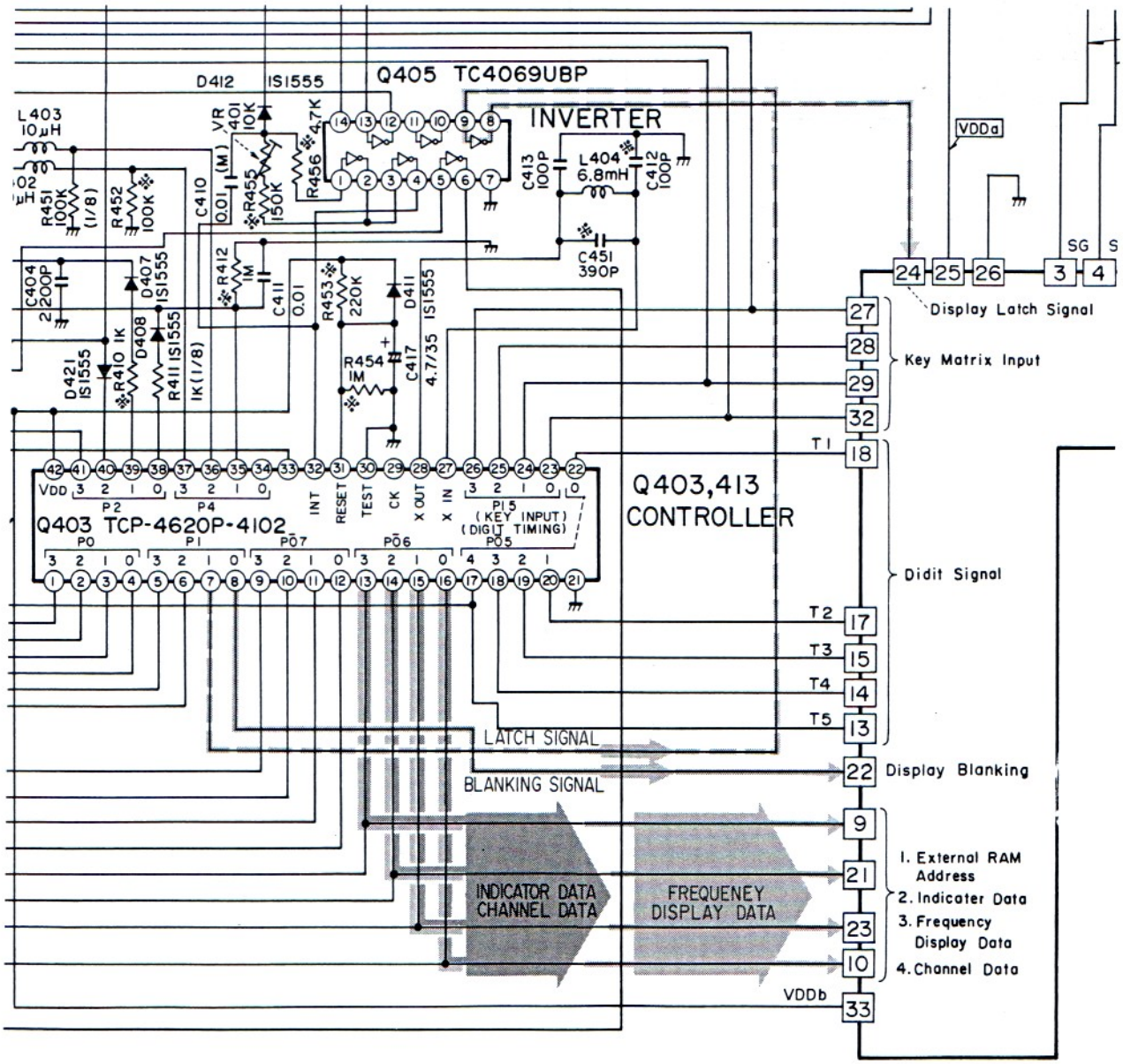
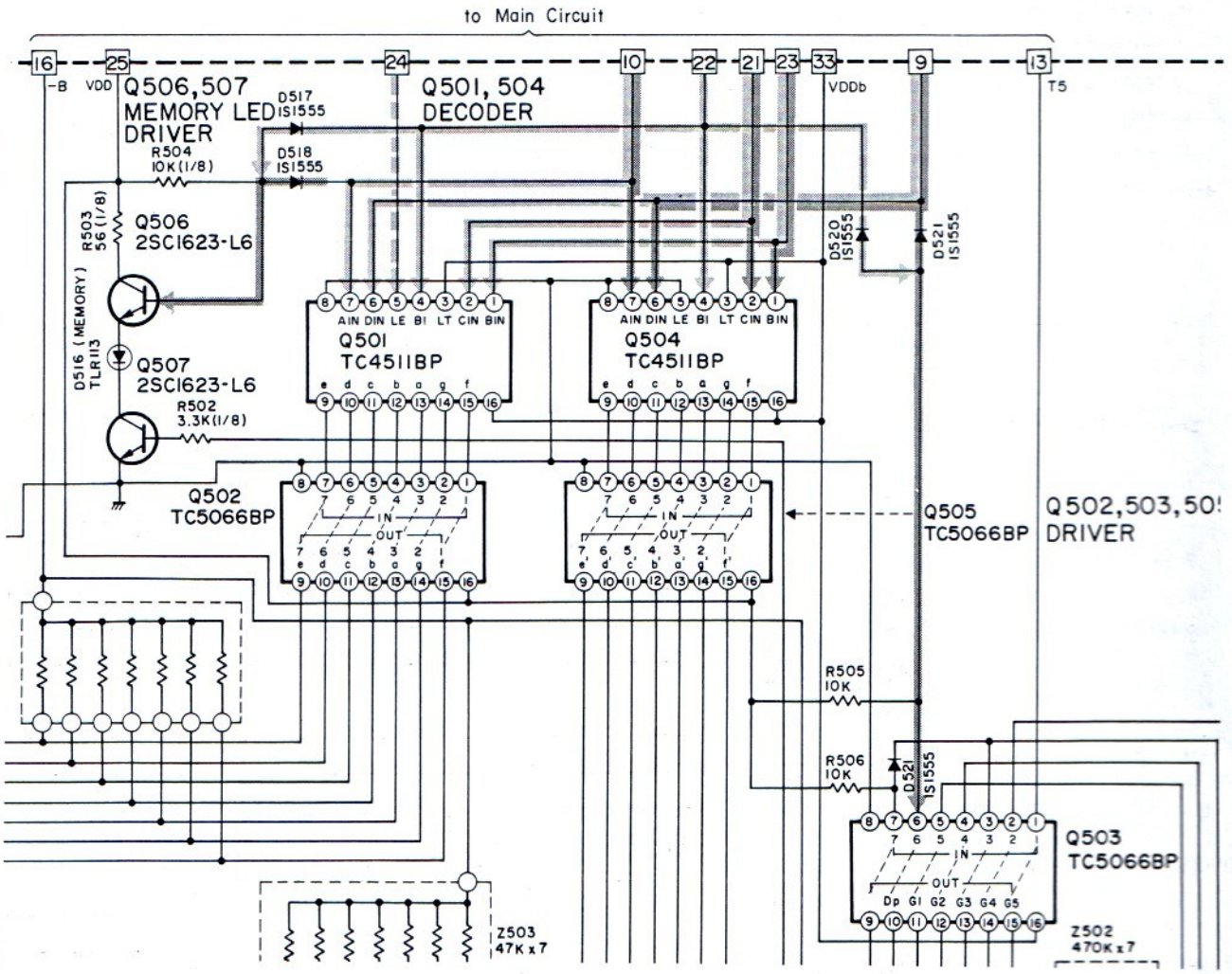


Figure 28.


to Main Circuit
16
25
24
10
22
21
23
33
9
13
-B
VDD
VDDb
T5
Q506,507
MEMORY LED
DRIVER
D517
IS1555
D518
IS1555
R504
10K(1/8)
R503
56(1/8)
Q506
2SC1623-L6
D516 (MEMORY)
TLR113
Q507
2SC1623-L6
R502
3.3K(1/8)
Q501, 504
DECODER
D520
IS1555
D521
IS1555
AIN DIN LE BI LT CIN BIN
Q501
TC4511BP
Q504
TC4511BP
Q502
TC5066BP
Q505
TC5066BP
Q502,503,505
DRIVER
IN
OUT
R505
10K
R506
10K
D521
IS1555
Q503
TC5066BP
Dp G1 G2 G3 G4 G5
Z503
47K x 7
Z502
470K x 7

8-3. Data Transfer to DISPLAY

- The output data to be transferred to the display is obtained from the PO6 ports (pin nos. (9) ~ (12)). The transfer of this data involves the transfer of the frequency display data and indicator data (channel display, memory display, D.P. etc.) in serial form within the respective $T_1 \sim T_5$ timing. This makes it necessary to employ a latched decoder in the display stage, and this is the role played by the TC-4511BP in the ST-S20.
- The timing chart employed is described here in greater detail (see Fig. 28 for corresponding circuit diagram).

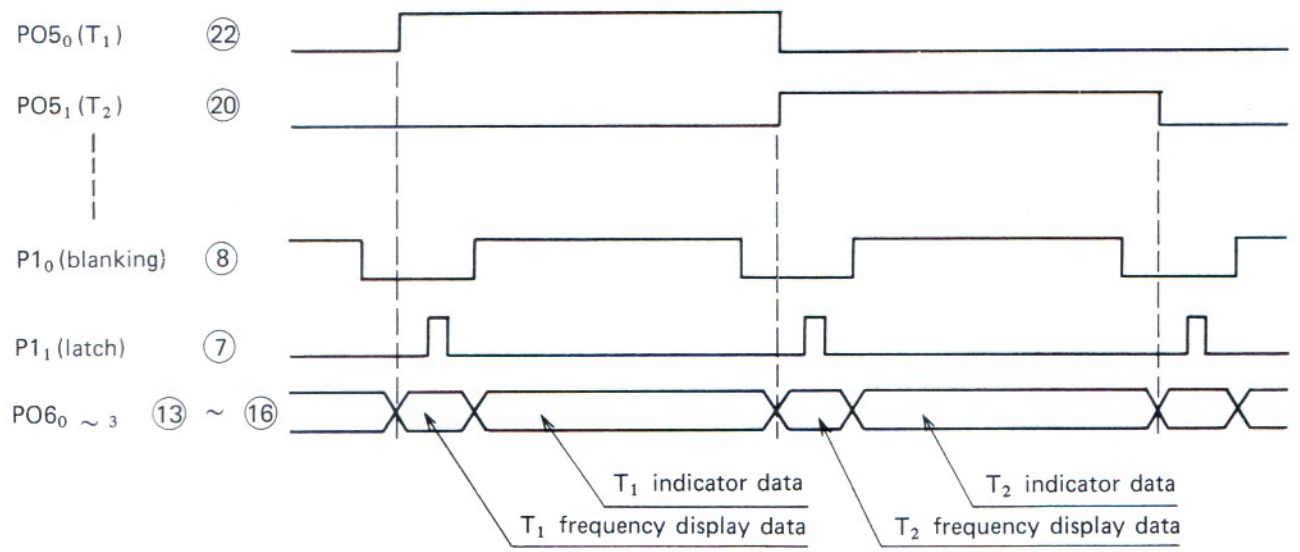


Figure 29.

- Data is transferred according to the following procedure.
  1. The display is first blanked out by the blanking signal from PI_0 (pin no. (8)).
  2. The frequency display output data is latched in the latched decoder (TC-4511BP) by the latch signal on pin no. (7).
  3. This is followed by output of the indicator data, resulting in the blanking being turned off for display of this data.
  4. At the same time that the indicator data is displayed in step 3, the frequency display data latched in step 2 is also displayed.
  5. Repeated transfer of this data proceeds in accordance to the respective $T_1 \sim T_5$ timing.
- Note that the PO7 ports (pin nos. (12) ~ (16)) normally handle this display output data, and is only switched over to RAM control data during RAM R/W operations. (See (2) on page 21.)
- Output of the indicator data occurs according to the following timing.

	T_1								T_3		T_4
$PO6_0$ (16)	1	0	1	0	1	0	1	0	1	0	0
$PO6_1$ (15)	0	1	1	0	0	1	1	0	0	0	0
$PO6_2$ (14)	0	0	0	1	1	1	1	0	0	0	0
$PO6_3$ (13)	0	0	0	0	0	0	0	1	0	1	1
Display contents	1CH	2CH	3CH	4CH	5CH	6CH	7CH	8CH	MEMORY	FM D.P.	SW D.P.

Figure 30.

8-4. Data Transfer to PLL

Transfer of data to the PLL involves conversion of the frequency channel data in the controller to PLL data (PLL programable counter values), which is then transferred as 4-bit serial data from the PO ports (pin nos. ① ~ ④). The PLL input data is controlled by the LOAD signal from pin no. ㊶ . Refer to section 5-5 for further details (and also refer to Figs. 6, 13 and 20).

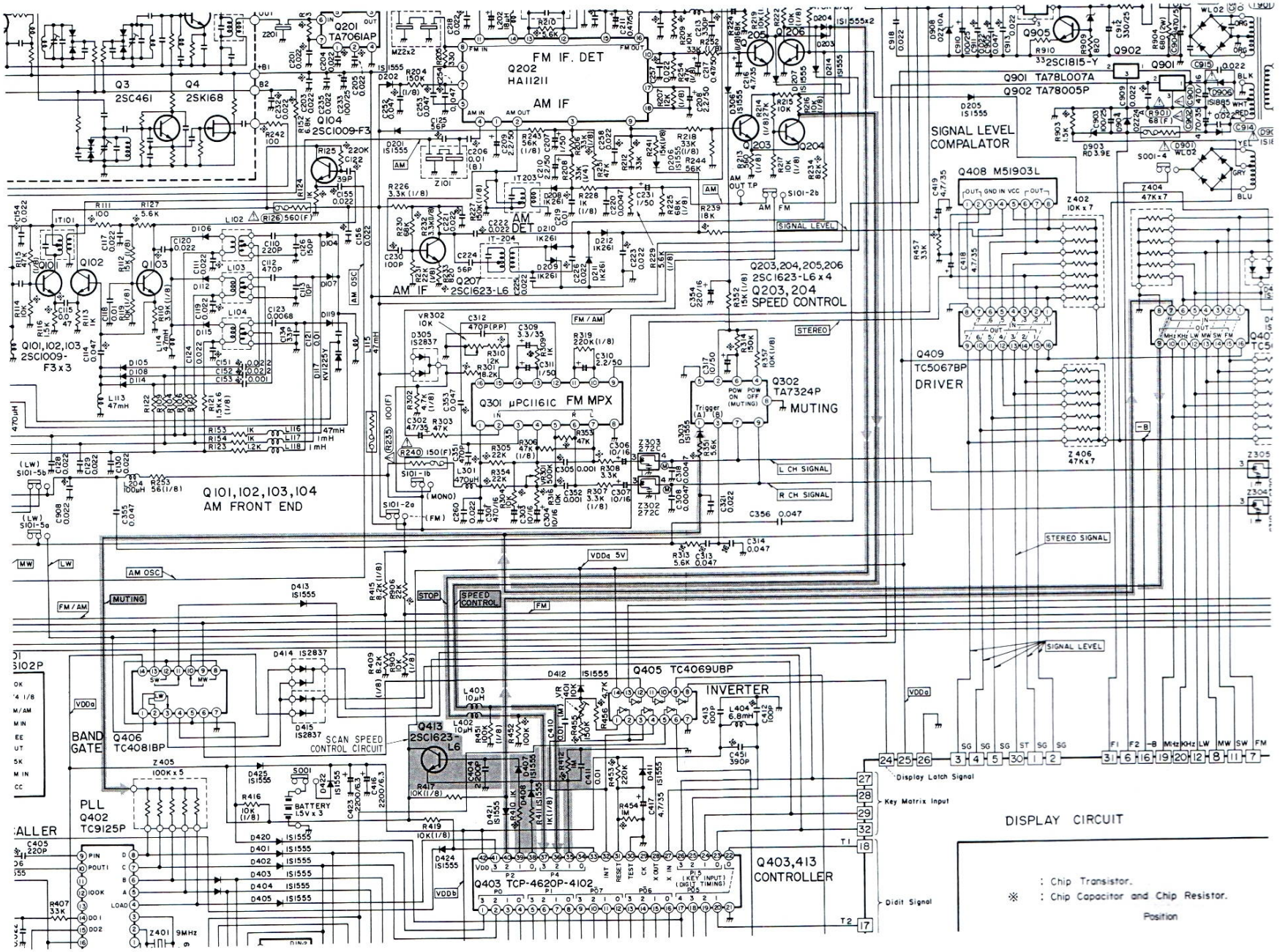

Q101,102,103 2SC1009-F3x3
Q101,102,103,104 AM FRONT END
Q104 2SC1009-F3
Q201 TA7061AP
FM IF. DET Q202 HA11211
AM IF
Q203,204,205,206 2SC1623-L6 x 4 Q203,204 SPEED CONTROL
Q207 AM IF 2SC1623-L6
Q301 μPC1161C FM MPX
Q302 TA7324P MUTING
Q303 2SC1623-L6
Q409 TC5067BP DRIVER
Q408 M51903L
SIGNAL LEVEL COMPALATOR
Q901 TA78L007A
Q902 TA78005P
Q402 TC9125P PLL
Q403 TCP-4620P-4102 Q403,413 CONTROLLER
Q405 TC4069UBP INVERTER
Q406 TC4081BP BAND GATE
SCAN SPEED CONTROL CIRCUIT
Q413 2SC1623-L6
DISPLAY CIRCUIT
: Chip Transistor.
※ : Chip Capacitor and Chip Resistor.
Position
Display Latch Signal
Key Matrix Input
Didit Signal
SIGNAL LEVEL
STEREO SIGNAL
L CH SIGNAL
R CH SIGNAL
AM OSC
MUTING
SPEED CONTROL
STOP
VDDa 5V
VDDa
VDDb
9MHz

Figure 31.

8-5. Auto Tuning Operation

The ST-S20 has been designed for automatic tuning operations in FM and MW bands.

- The timing chart involved when the [AUTO] key is pressed and the corresponding input signal is applied to the controller, is shown in the following diagram.

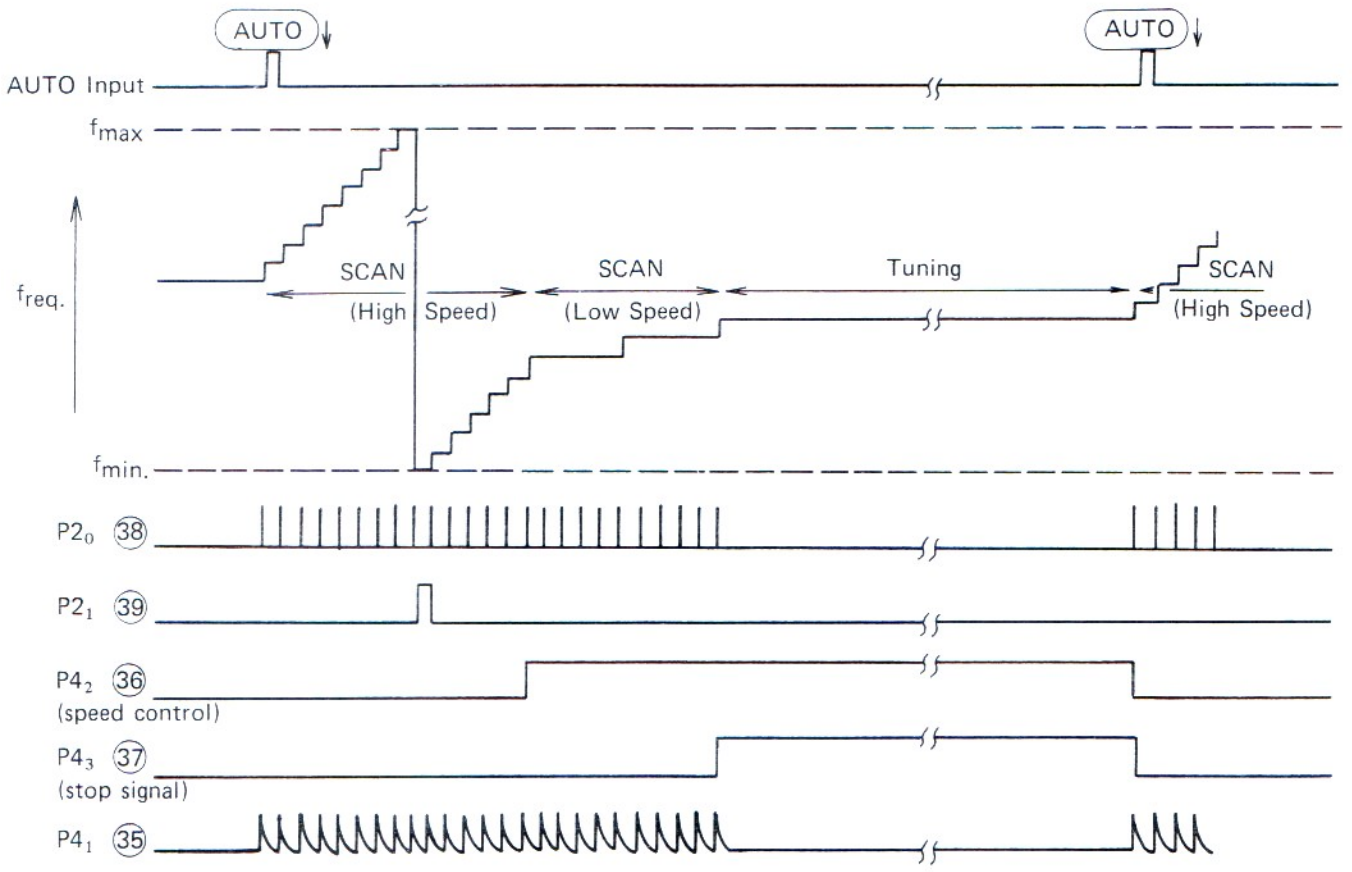


Figure 32.

During the following description, also refer to the circuit diagram in Fig. 31.

- When the [AUTO] key is pressed, the controller counter starts to count up (i.e. the reception frequencies are changed sequentially in the upward direction).
- The scanning speed at this time is determined by the values of C and R connected to pin nos. (39), (38) and (35).
- Once the maximum reception frequency (f_{max}) is reached, the scanning mechanism scans back towards the minimum reception frequency (f_{min}).
- When the frequency of a broadcasting station is approached, the speed control terminal (pin no. (36)) is switched to "1", resulting in the scanning speed being slowed down (the slower speed being determined by internal time constants – normally slowed to about 1/5 of scanning speed).
- At the tuning point, a stop signal is applied to pin no. (37), resulting in the counting being stopped.

- Also note that during the frequency scanning process, a muting signal is obtained from $P2_2$ (pin no. (40)) to prevent the output of any sound. 0.5 seconds after reaching the tuning point, the muting circuit is switched off to permit the output of sound.
- This scanning operation can also be achieved by depressing the [UP] or [DOWN] key for more than 1 second without pressing the [AUTO] key. In this case, however, frequency scanning will only continue as long as the [UP] or [DOWN] key is depressed. Nor is there any scanning speed control.
- In the SW and LW positions, a stop signal is applied continuously to $P4_3$ (37) , thereby stopping the frequency scanning operation after each step.

  Note: Although LW frequencies are normally changed in 1 kHz steps, the frequencies are scanned in 9 kHz steps when the [AUTO] key is pressed. This is because the IC has been designed to accept the stop signal only at frequencies of 9N + 2 (Hz) (where N is always an integer).

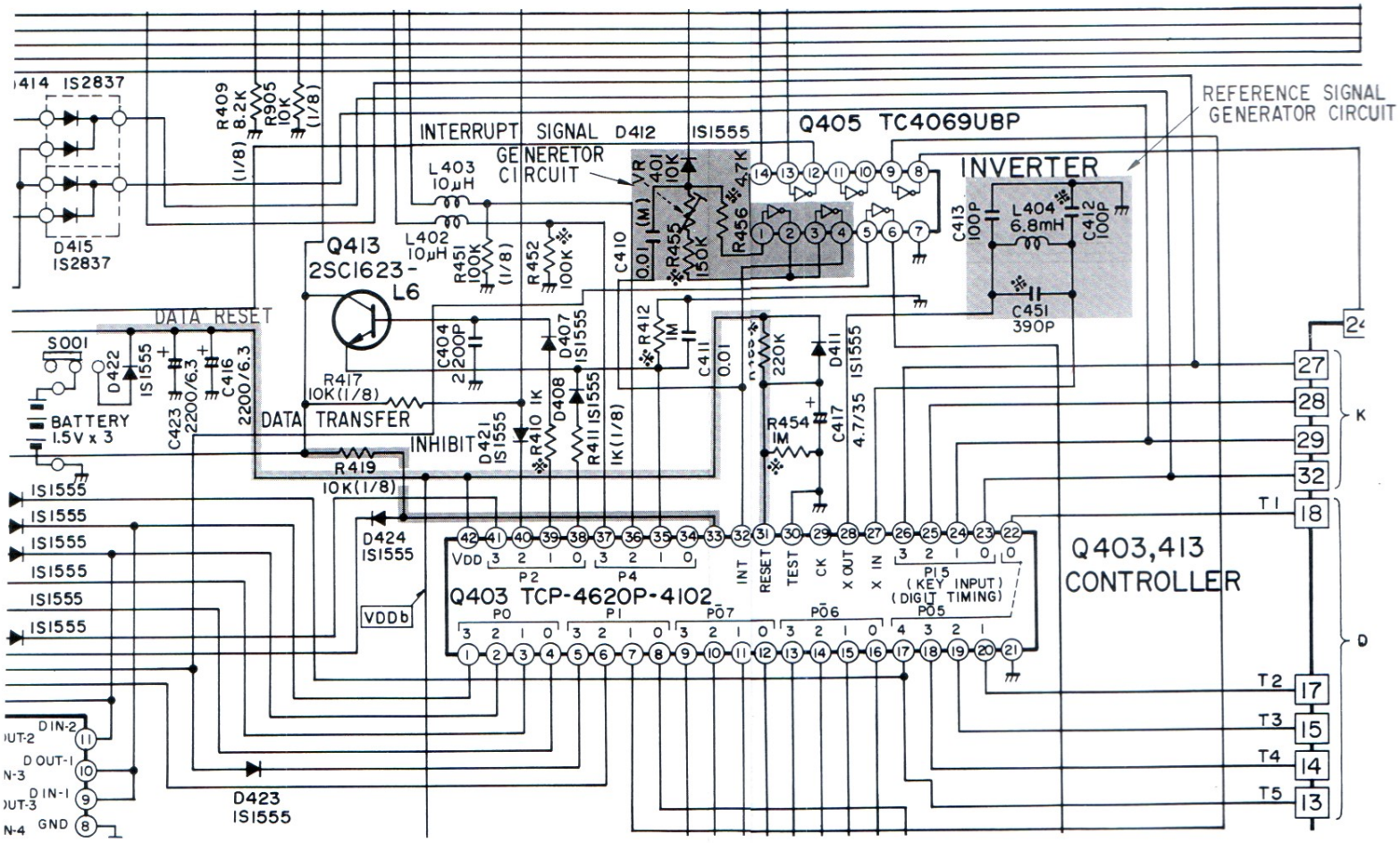

REFERENCE SIGNAL GENERATOR CIRCUIT
INTERRUPT SIGNAL GENERETOR CIRCUIT
Q405 TC4069UBP
INVERTER
Q403,413 CONTROLLER
Q403 TCP-4620P-4102
DATA RESET
DATA TRANSFER
INHIBIT
BATTERY 1.5V x 3
Q413 2SC1623-L6
D412 IS1555
D415 IS2837
D424 IS1555
D423 IS1555
VDDb
L403 10μH
L402 10μH
L404 6.8mH
C451 390P
R417 10K(1/8)
R419 10K(1/8)
R454 1M
C417 4.7/35
D411 IS1555
D407 IS1555
D408 IS1555
D421 IS1555
R410 1K
R411 1K(1/8)
C404 2200P
C410 0.01
C411 0.01
R412 1M
R456 47K
R455 150K
R452 100K
R451 100K(1/8)
R409 8.2K(1/8)
R905 10K(1/8)
C413 100P
C412 100P
C423 2200/6.3
C416 2200/6.3
S001
D422 IS1555
P2
P4
P15 (KEY INPUT) (DIGIT TIMING)
P0
P1
P07
P06
P05
VDD
INT
RESET
TEST
CK
X OUT
X IN
DIN-2
DOUT-1
DIN-1
GND
T1
T2
T3
T4
T5
K
D

Figure 33.

8-6. Other Functions and Circuits

Other controller functions and corresponding circuits are described briefly below. (See Fig. 33)

Interrupt signal generator circuit

This oscillator circuit composed of 2 inverters and a CR circuit is located in TC-4069. The input signal is applied to pin no. (32) .

Reference signal generator circuit

This LC oscillator circuit oscillates at a frequency of 100 kHz, the input signal being applied to pin nos. (27) and (28) .

Data transfer inhibition

When pin no. (33) is switched to "L" level, data transfer to the PLL IC (TC-9125P), and read out from and write in to the MEMORY IC (TC-5501P) are all inhibited.

Data reset

When pin no. (31) is switched from "L" to "H", the IC counter is reset to a predetermined initialization status (listed below).

Band	IC Channel Data	PLL Data	Reception Frequency
FM	28	1000	89.30 MHz
SW	750	2000	9.550 MHz
MW	91	200	1350 kHz
LW	95	700	250 kHz

Figure 34.

Appendix

PLL data N and controller channel data N' are calculated from the reception frequency f (see Fig. 6) in the following way.

FM: $N_{FM} = \frac{f(MHz) + 10.7}{8 \times 0.0125} = 10\ (f(MHz) + 10.7)$, $N'_{FM} = N_{FM} - 982$

SW: $N_{SW} = \frac{f(MHz) + 0.45}{0.005} = 200\ (f(MHz) + 0.45)$, $N'_{SW} = N_{SW} - 1250$

MW: $N_{MW} = \frac{f(kHz) + 450}{9} = 1/9\ (f(kHz) + 450)$, $N'_{MW} = N_{MW} - 109$

LW: $N_{LW} = \frac{f(kHz) + 450}{1} = f(kHz) + 450$, $N'_{LW} = N_{LW} - 605$

Note: The above formula for FM can only be used when the FM frequency display is [ ][ ][ ][0]. For 50 kHz displays, the f value is obtained by subtracting 0.05 MHz from the reception frequency (this corresponds to the 50 kHz shift described in section 4-3 on the prescaler).

Precautions in Handling Pierced Type PC Boards

This diagram is an outline of the general structure of the pierced holes in the PC boards employed in the ST-S20.

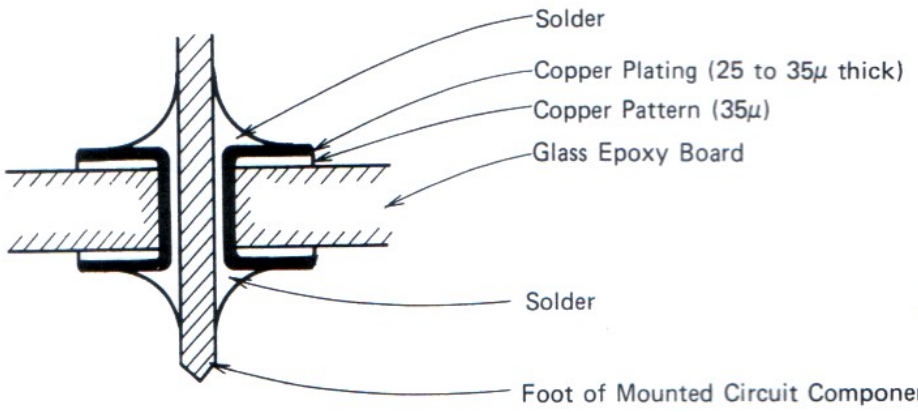


Figure 35.

- As the diagram shows, the copper pattern on both sides of the hole in pierced type PC boards is connected by a layer of copper plating.
- The main point to remember when replacing circuit components is that these copper plated holes must not be drilled out or processed in any way.
- If the hole has been blocked with solder, use a solder remover and soldering iron to clear the hole of excess solder.

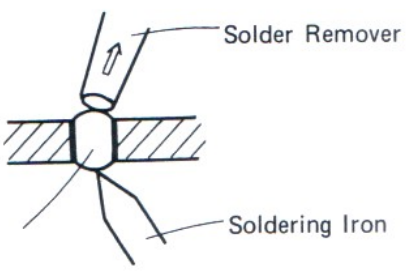


Figure 36.

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